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APPLICATION

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TITLE: CREATING SHALLOW JUNCTION TRANSISTORS

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CREATING SHALLOW JUNCTION TRANSISTORS

Background

This invention relates generally to forming semiconductor integrated circuits.

Semiconductor integrated circuits may include metal oxide semiconductor field effect transistors (MOSFETs) having a gate, source and drain. The fundamental driver of the electronics industry is transistor scaling. For the last 30 years, this has followed the trend of scaling transistor dimensions by 0.7X per process generation. This also requires that the shallow source/drain extensions be scaled by this geometric factor in order to not degrade the transistor performance.

Ideally, the shape and resistivity of the source drain extension needs to be preserved. Resistivity is maintained on a shallower junction by increasing dopant dose and activation. Increased dopant activation is achieved with advanced annealing technologies that anneal at higher temperatures in a shorter period of time. These annealing techniques are optimized to yield the correct amount of dopant diffusion and activation. As the junctions are scaled, the trend is towards lower thermal budgets for the anneal.

Traditionally, the junction depth has been scaled by reducing the diffusion time rather than the implant energy. The implant energy has been harder to scale because of an incompatability with the clean process used in semiconductor manufacturing. Dopants near the surface are removed during the clean process. In addition, there are implant tails and straggle that can impact the final shape of the source drain extension. Eventually, this will lead to a distortion of the shape of the source and drain extension shape.

Another component of the junction scaling is implant damage. The anneal step typically removes the defects. As the total amount of thermal energy is reduced to scale the junction, the residual damage can increase. This can have negative impact on the dopant activation. Novel transistor designs on fully depleted silicon over insulator (FDSOI) will have problems with recrystalization on oxide if the thin layer of silicon is amorphized. As gate oxides are scaled, the thinner film may be degraded more adversely by implant straggle and angular divergence.

One approach to reducing this damage involves applying doped glass followed by a diffusion drive-into form the junctions. The advantage of the doped glass method is that lattice damage is minimized and there is no implang damage. The limitation of this technique is that the peak concentration of dopants at the interface is lower than

desirable for the modern complementary metal oxide semiconductor (CMOS) process.

Plasma doping enables doping at energies significantly lower than those of conventional implants and semiconductor processes. The substrate to be doped is placed directly in the plasma source while applying a bias to the substrate. Generally plasma doping is done at energy ranges of 200ev to 5 keV. Ultra low energy plasma doping below 200ev down to 10 eV have been attempted but have not been effectively integrated into transistor processes because of the incompatability with the clean process.

Thus, there is a need for better ways to form shallow junctions transistors.

Brief Description of the Drawings

Figure 1 is a partial, enlarged schematic cross-sectional view of initial stage in the manufacture of a shallow field effect transistor in accordance with one embodiment of the present invention;

Figure 2 is an enlarged, schematic cross-sectional view at a subsequent stage in the manufacture of a shallow junction transistor in accordance with one embodiment of the present invention;

Figure 3 is an enlarged, schematic cross-sectional view at a subsequent stage in the manufacture of a shallow junction transistor in accordance with one embodiment of the present invention; and

Figure 4 is an enlarged, schematic cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention.

Detailed Description

Using conventional techniques, a gate structure 16 may be defined over a semiconductor substrate 12 with an intervening gate dielectric 14 as shown in Figure 1. The gate structure 16 may use polysilicon, silicide, or metal, as examples. This invention is not limited to the traditional CMOS structure and is applicable to novel structures such as the "fin-fet" or the "tri-gate" transistors. Also, the sequence describes formation of a PMOS source/drain extension after the NMOS junction implant. This invention may simultaneously be applied to the NMOS in the same process flow. Because of the differential junction requirements for NMOS and PMOS, an intermediate diffusion step after the NMOS junction implant/cap is used to separately adjust the NMOS junction. The final anneal step to diffuse both NMOS and PMOS will occur later in the process flow.

In one embodiment of the present invention, the wafer 10 is a complementary metal oxide semiconductor (CMOS) wafer with the structure 16 ultimately acting as the gate electrode of a PMOS transistor. At this stage, the NMOS transistor (not shown) may be covered with an appropriate resist or other protective covering.

Referring to Figure 2, the PMOS structure may then be subjected to plasma doping to form the source/drain extensions of a graded source/drain junction. In one embodiment, the angular divergence of the plasma beam may be adjusted such that the sidewalls 17 of the gate structure 16 are doped to substantially the same extent as the upper wall 19. Thus, a fairly evenly shaped doped region 20 may be formed on the top and sides of the polysilicon structure 16 in one embodiment of the present invention.

At the same time, shallow implanted regions 18 may be formed adjacent the edges of the gate structure 16 corresponding to what ultimately will become the source and drain regions. Plasma doping may be accomplished using a variety of techniques including boron plasma doping to control the angular divergence of the dopants. The plasma doping may be accomplished at energies below 200eV down to 10 eV in one embodiment.

In one embodiment of the invention, after the doping process, the NMOS resist is removed with a resist ash process. Afterwards, the surface is cleaned with a hydrogen plasma instead of the traditional wet clean. The use of hydrogen plasma to clean surfaces may be highly effective in removing contaminants that may interfere with subsequent shallow junction formation. The entire wafer is then capped with a protective layer that will remain on the

wafer until a spacer is added to the sides of the polysilicon gate. The uncovered region is then removed.

Alternately, the NMOS resist can be left on immediately after the doping process. A low temperature CVD process can deposit a silicon film on top of both the NMOS resist area and the exposed, doped PMOS region. In a yet to be determined process, the silicon film and photoresist on the NMOS region is removed. This can be followed by either a wet clean or a dry hydrogen plasma.

In third embodiment of the present invention, the NMOS and PMOS regions may be doped without any use of photoresist in a blanket doping process and then capped. The cap layer may be deposited and then patterned to expose the NMOS area. If the dopant deposited is very shallow, then it may be removed from the NMOS region in a subsequent clean operation.

The capping layer 22 needs to be deposited in a low temperature process to avoid diffusing the junctions. An example of a material would be a CVD doped glass or silicon.

The remainder of the processing of the PMOS transistor may be completed, to the extent possible, with the capping layer 22 in place. The presence of the capping layer 22 reduces the removal of surface doping, particularly in subsequent clean processes. Using the protective capping layer 22, a very thin layer of a doping may be achieved

having relatively high surface concentrations of doping with significantly reduced implant damage given the very low energies involved in some embodiments.

The cap layer is to remain until the spacer is deposited on the gate side walls. After this step, the cap layer directly beneath the spacer will be protected from subsequent cleans. Beyond the spacer, the cap layer can be removed if required. This depends on the composition of the cap layer and whether there are any processing problems downstream (ex. Salicide, implant knock-in for the source/drain implant).

Thereafter, as indicated in Figure 4, rapid thermal annealing may be utilized to diffuse the junctions to the desired depth. Diffusion dominates the final junction depth rather than the plasma doping itself. The final junction, as indicated at 18a, and the final doping within the polysilicon structure 16, as indicated at 20a, may be effective to form low damage, shallow PMOS transistor junctions. Diffusing the dopant from a high concentration at the surface will serve to increase the amount of dopant in the source/drain extension immediately underneath the polysilicon gate edge.

The use of conformal doping techniques, such as plasma doping and immersion plasma doping, may result in a reduction in the depletion depth in the polysilicon gate electrode in the structure 16 close to the gate edge. This

improved polysilicon depletion enables the scaling of the source/drain underdiffusion while maintaining the same overlap capacitance and transistor performance and allowing more aggressive polysilicon gate electrode scaling. As a lateral doping depth becomes comparable to a significant fraction of the polysilicon critical dimension, polysilicon depletion may be reduced.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: